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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
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6

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/002,405	Applicant(s) EDLIS ET AL.
	Examiner James C Kerveros	Art Unit 2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☒ Claim(s) *1-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings are required in this application because of improper character size used in FIGS. 1-4. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because it lacks proper language.

On lines 1, and 4 the term "may be" should be changed to "is". Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claims 1-18 are objected to because of the following informalities:

Appropriate correction is required.

Claims 1-18 require indentation. Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(m).

Claims 1-6 and 13, a colon ":" should be inserted following the transitional term "comprising", to be consistent with the rest of the claims.

Claim 5, on line 1, "claim 5" should be changed to "claim 4".

Claim 18, on line 1, "claim 19" should be changed to "claim 17".

Claim 5, on line 1, "the first .....output" lacks antecedent basis.

Claim 3, on line 2, "an output" should be changed to a "first output" to correct the antecedent basis of claim 5.

Claim 4, on lines 2 and 4, "second block" should be changed to "second sub-block".

Claim 6, on line 2, "second block" should be changed to "second sub-block" and on line 3, "first block" should be changed to "first sub-block".

Claim 14, on line 3, "second block" should be changed to "second sub-block".

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 14, 15 and 27-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 27, the phrase "may be" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Regarding Claim 14, similarly the term "may" renders the claim indefinite for the same reason cited for claim 27, above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 17, 18, 19, 24-30 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viterbi et al. (US 5933462).

Regarding independent Claim 17 and dependent 18, Viterbi substantially discloses a processor 28 having digital memory and a memory controller adapted to provide a forward iterative calculator corresponding to results from decoder 24 and a backward iterative calculator corresponding to results from decoder 26.

However, Viterbi does not explicitly disclose a memory unit comprised of a digital memory and a memory controller adapted to provide a forward iterative calculator and a backward iterative calculator simultaneous access to the memory. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use processor 28 having digital memory and a memory controller, as taught by Viterbi, for accessing the results from the forward and backward Viterbi decoders (24, 26) and

for storing the iterative calculations from the corresponding first and second sub-blocks, since it is cost effective to use an already existing memory with its associated controller, which is inherent in a processor.

Regarding independent Claims 19 and 30, Viterbi substantially discloses an apparatus and method for decoding an encoded block of data from a convolutional encoder (12), using soft decision output decoder (20), FIG. 3, including parsing the encoded data block (12) into a first sub-block decoder (20) corresponding to a first processing unit to perform forward and backward decoding using Viterbi decoders (24, 26), which are part of output decoder (20), FIGS. 3, 4. Further, Viterbi discloses a processor 28 including memory for storing the results from the Viterbi decoders (24, 26).

Viterbi does not explicitly disclose a second processing unit to perform forward and backward decoding on a second sub-block. However, Viterbi discloses the identical method step of performing forward and backward iterative calculations on a first sub-block using forward and backward Viterbi decoders (24, 26), FIG. 4. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the forward and backward Viterbi decoders, as taught by Viterbi, to perform forward and backward iterative calculations on a second sub-block, since the iterative calculations are identical as the first sub-block.

Regarding Claims 24-26 and 34, Viterbi does not explicitly disclose a temporary memory including the steps of storing the results of the iterative calculation of the second sub-block on a temporary memory on which results from the iterative calculation of the first block are stored, and wherein results from the iterative calculations on the

second sub-block are stored to a portion of the temporary memory after an output based on results stored in that portion of memory is calculated. However, Viterbi discloses processor 28 including memory for storing the results from the Viterbi decoders (24, 26). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the memory processor 28, as taught by Viterbi, to store the iterative calculations from a first and second sub-blocks, since it is cost effective to use an already existing memory of the processor.

Regarding Claim 27, Viterbi discloses in FIG. 5, a trellis diagram of a blocked convolutional code, showing forward and backward recursions partitioned into two or more segments corresponding to nodes.

Regarding Claims 28, 29 and 32, Viterbi does not explicitly disclose the steps, where the sub-block segments are decoded by a separate process running on one of the processing unit and on a digital signal processor. However, Viterbi discloses separate decoders (24, 26), which are run separately corresponding to separate processing units. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use decoders (24, 26), as taught by Viterbi, for processing separate segments, such as nodes, as shown by the trellis diagram.

Regarding Claim 33, Viterbi does not explicitly disclose the step of combining the first and second output into a single data block. However, Viterbi employs processor 28 for combining the results of forward and backward iterative calculations from the Viterbi decoders (24, 26), where the first output is recited in claim 3 above. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to

combine the second output at the processor 28 of Viterbi, since the processor already accepts the first output.

7. Claims 1-16, 20-23 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viterbi et al. (US 5933462) in view of Lee et al. (US 6289486).

Regarding independent Claims 1 and 8, Viterbi substantially discloses a method and apparatus for decoding an encoded block of data from a convolutional encoder (12), using soft decision output decoder (20), FIG. 3, comprising:

A data block in encoder (12), such as a first sub-block assigned to forward and backward Viterbi decoders (24, 26), FIG. 4. Performing backward iterative calculations on the first sub-block using backward Viterbi decoder 26, which initiates a backward recursion through the trellis, based on data from the encoder (12) and (step 64, FIG. 7).

Viterbi does not explicitly disclose a second sub-block for performing backward iterative calculations on the first sub-block "based on results from backward iterative calculations on a portion of the second sub-block".

However, Lee discloses a sub-block diagram (FIG. 4) of a turbo decoder for decoding the output of the serial turbo encoder shown in FIG. 2, which includes a first decoder 11 corresponding to a first sub-block and a second decoder 14 corresponding to a second sub-block. The output results from the second decoder 14 is fed to the input of the second decoder 11 through interleaver 13. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the output results from the second sub-block decoder 14, as taught by Lee, in the first sub-

block assigned to the backward Viterbi decoder (26) of the Viterbi reference, for the purpose of performing backward iterative calculations on the first sub-block based on the results from the second sub-block, so a to enhance performance characteristics in terms of bit error rate by repeatedly decoding input data, using an iterative decoding algorithm.

Regarding Claims 2, 9 and 21, Viterbi discloses performing forward iterative calculations on the firsts sub-block encoder (12) using forward Viterbi decoder 24 and (step 60, FIG. 7).

Regarding Claims 20 and 31, Viterbi does not explicitly disclose a first processing unit that is able to perform a backward iterative calculation on at least a portion of the first sub-block based on results of a backward iterative calculation performed by the second processing unit on at least a portion of the second sub-block.

However, Lee discloses a sub-block diagram (FIG. 4) of a turbo decoder for decoding the output of the serial turbo encoder shown in FIG. 2, which includes a first decoder 11 corresponding to a first sub-block and a second decoder 14 corresponding to a second sub-block. The output results from the second decoder 14 is fed to the input of the second decoder 11 through interleaver 13. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the output results from the second sub-block decoder 14, as taught by Lee, in the first sub-block assigned to the backward Viterbi decoder (26) of the Viterbi reference, for the purpose performing backward iterative calculations on the first sub-block based on the results from the second sub-block, so a to enhance performance characteristics in

terms of bit error rate by repeatedly decoding input data, using an iterative decoding algorithm.

Regarding Claims 3, 10 and 22, Viterbi discloses calculating an output (Ut) at the dual maxima processor 28 based on the results of forward and backward iterative calculations corresponding to Viterbi decoders (24, 26), FIG. 4.

Regarding Claims 4, 11 and 23, Viterbi does not explicitly disclose performing forward and backward iterative calculations on the second sub-block and calculating a second output based on such results. However, Viterbi discloses the identical method step of performing forward and backward iterative calculations on a first sub-block using forward and backward Viterbi decoders (24, 26), FIG. 4. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the forward and backward Viterbi decoders, as taught by Viterbi, to perform forward and backward iterative calculations on the second sub-block, since the iterative calculations are identical as the first sub-block.

Regarding Claim 5, Viterbi does not explicitly disclose the step of combining the first and second output into a single data block. However, Viterbi employs processor 28 for combining the results of forward and backward iterative calculations from the Viterbi decoders (24, 26), where the first output is recited in claim 3 above. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the second output at the processor 28 of Viterbi, since the processor already accepts the first output.

Regarding Claims 6, 7 and 13-16, Viterbi does not explicitly disclose a temporary memory including the steps of storing the results of the iterative calculation of the second sub-block on a temporary memory on which results from the iterative calculation of the first block are stored, and wherein results from the iterative calculations on the second sub-block are stored to a portion of the temporary memory after an output based on results stored in that portion of memory is calculated. However, Viterbi discloses processor 28 including memory for storing the results from the Viterbi decoders (24, 26). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the memory processor 28, as taught by Viterbi, to store the iterative calculations from a first and second sub-blocks, since it is cost effective to use and already existing memory of the processor.

Regarding Claim 12, the processing unit comprises a forward iterative calculator Viterbi decoder 24, a backward iterative calculator Viterbi decoder 26 and an output calculator processor 28.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
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Date: 13 May 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

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